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METHOD AND STRUCTURE FOR PROVIDING TUNED LEAKAGE CURRENT IN CMOS INTEGRATED CIRCUITS

Abstract

A method and structure for tuning a threshold voltage of nFET and pFET devices in a double-gate CMOS integrated circuit structure, wherein the method comprises performing a PSP (post silicide processing) electrical test on the double-gate CMOS integrated circuit structure, determining nFET and pFET threshold voltages during the PSP test, and implanting the double-gate CMOS integrated circuit structure with an alkali metal ion, wherein the step of implanting adjusts the nFET and pFET threshold voltages by an amount required to match desired off-currents for the nFET and pFET devices. According to the method, prior to the step of performing, the method comprises forming a fin structure over an isolation layer, forming source/drain regions over the fin structure, depositing a gate oxide layer adjacent to the source/drain regions, and forming a gate region over the gate oxide layer and the fin structure. The metal ion comprises any of cesium and rubidium.